Request for Extension of Time

This is supplemental to the response send on July 5, 2005, and, if necessary, Applicants hereby request an extension of time of two months to September 5, 2005 to respond to the Office Action of April 5, 2005. The Commissioner is hereby authorized to charge any additional fees for this extension of time due or credit any overpayment to Deposit Account No. 50-2421.

Remarks/Arguments

With reference to the Office Action mailed April 5, 2005, Applicants offer the following remarks and argument.

Status of the Claims

Claims 1 to 20 were originally presented for examination. All of the claims were subject to a restriction requirement, with Claims 4, 7-8, 10, 13, and 16-17 deemed to be directed to Species I, and Claims 1-3, 5-6, 9-12, 14-15, and 18-20 deemed to be directed to Species II.

Applicants have previously elected to pursue the invention of Species II and have canceled Claims 4, 7-8, 13, and 16-17.

The claims now pending are claims 1-3, 5-6, 9-12, 14-15, and 18-20.

Office Action of April 5, 2005

Claims 1-3, 5-6, 9-11, 14-15, and 18-20 were rejected under 35 USC 102(b) as being anticipated by US Patent 5,973,337 to Knapp et al., citing column 1, line 61 to column 3, line 4[1], and column 3, lines 19-30[2]

[1] Column 1, line 61 to column 3, line 4-

FIG. 1 illustrates a cross-sectional view of a portion of a semiconductor or optoelectronic device 10 in accordance with an embodiment of the present invention. Semiconductor device 10 is comprised of a substrate 11 having conductive traces 12 and solder pads 13 disposed on a bottom surface of substrate 11 and conductive traces 14 and a chip or die attach pad 17 disposed on a top surface. Solder pads 13 are also referred to as interconnect pads. Substrate 11 is also referred to as a ball grid array substrate. Chip attach pad 17 serves as a semiconductor chip receiving area. Suitable materials for substrate 11 include resins, such as epoxy, polyimide, aramide, triazine, or a phenolic resin, as well as epoxy-glass composites, Printed Circuit Board (PCB) materials, FR-4, FR-5, ceramics, and the like. Preferably, substrate 11 is Bismaleimide Triazine (BT) resin. By way of example, conductive traces 12 and 14, solder pads 13, and chip attach pads 17 are formed by laminating a conductive foil to the top and bottom surfaces of substrate 11. Conductive traces 12 and 14, solder pads 13, and chip attach pads 17 are defined by patterning the conductive foil using lithographic techniques.

Alternatively, conductive traces 12 and 14, solder pads 13, and chip attach pads 17 may be screen printed or otherwise deposited onto the surfaces of the substrate. Subsequently, conductive traces 12 and 14, solder pads 13, and chip attach pad 17 are typically plated with gold or a combination of gold and nickel to form a non25 oxidizable surface for wirebonding and attaching solder balls 18. Although conductive traces 12 and 14, solder pads 13, and chip attach pad 17 have been described as comprising two conductive layers, it should be understood that the number of conductive layers and the materials of the conductive layers is not a limitation of the present. It should be further understood that for purposes of clarity conductive traces 12 and 14, solder pads 13, and chip attach pads 17 are illustrated as being a single layer of material throughout the description of the invention. Further, the number of conductive traces 12 and 14 and solder pads 13 is not a limitation of the present invention.

Conductive vias 19 are typically formed in substrate 11 by drilling or punching vias or holes through solder pads 13, substrate 11, and conductive traces 14. Subsequently the vias are plated with an electrically conductive material 21 such as, for example, copper. Other suitable materials for plating the holes include gold, nickel, a combination of gold and nickel, and the like.

The exposed portions of the top surface of substrate 11, conductive traces 14, and chip attach pad 17 are covered with a layer 22 of solder mask material. Solder mask layer 22 covers the ends of conductive vias 19 at the top surface of substrate 11.

Then the bottom surface of substrate 11 is coated with an insulating material such as, for example, liquid solder mask material 23 using, for example, a screen printing technique. Preferably, solder mask material 23 fills conductive vias 19. Suitable materials for liquid solder mask material 23 include photoresist, polyimide, or the like. Although solder mask material 23 is shown as filling conductive vias 19, it should be understood this is not a limitation of the present invention. In other words, solder mask material 23 may partially fill conductive vias 19. Solder mask material 23 is cured after filling conductive vias 19.

Semiconductor device 10 further comprises a semiconductor component such as a semiconductor chip 24 coupled to die attach pad 17 via a die attach material 25 such as, for example, a silver filled epoxy. Semiconductor chip 24 is also referred to as an integrated circuit or semiconductor die. Other suitable die attach materials include rubbers, silicones, polyurethanes, and thermoplastics. Semiconductor chip 24 is preferably an optoelectronic component or photonic device containing optically active portions such as vertical cavity surface emitting lasers (VCSEL), light emitting diodes, laser diodes, edge-emitting diodes, charge coupled devices (CCDs), complementary metal oxide semiconductor (CMOS) image sensors, and other light detection devices. Thus, semiconductor chip 24 may be an optical detection device or an optical reception device.

[2] Column 3, lines 19-30 –

Semiconductor chip 24, interconnect wires 27, and a portion of solder mask layer 22 are covered by an optically transmissive material such as an optically transmissive potting material 29, which is then cured. Potting material 29 is applied using techniques such as dispensing, transfer molding, injection molding, and

Claims 1-3, 5-6, 9-11, 14-15, and 18-20 were also rejected under 35 USC 102(e) as being anticipated by US Patent 6,627,872 to Fukamura et al., citing Column 1, lines 34-65[3], Column 6, line 63, to Column 7, line 36[4], Column 8, lines 26-31[5], and Column 9, lines 11-40[6],

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the like. The passivation layer (not shown) and lenslets 28 are sensitive to heat as well as being susceptible to oxidation. Therefore, potting material 29 protects the passivation layer and lenslets 28 formed on semiconductor chip 24 from damage by heat and oxidation, among other things.

[3] Column3, lines 33-65

Referring now to FIGS. 20(a) and 20(b), the semiconductor optical sensing apparatus includes a detecting section and an optical section. The detecting section includes a semiconductor optical sensor chip 111, a ceramic casing 112, lead frames 113, bonding wires 114 and a transparent plate 116. The sensor chip 111 is die-bonded to the casing 112. The lead frames 113 include lead pins. The bonding wires 114 connect the internal terminals of the sensor chip 111 and the lead frames 113. The transparent plate 116 is fixed to the open end of the casing 112 with a layer 115 of glass having a low melting point or of adhesive.

The sensor chip 111 is mounted on the inner bottom face of the casing 112 and sealed in the casing 112 by the transparent plate 116. The space enclosed by the casing 112 and the transparent plate 116 is filled with a transparent filler (not shown) or with gas. The detecting section is fixed to a printed circuit board 117 by soldering the lead frames 113 to the printed circuit board 117.

The optical section includes an aspherical glass lens 118, a lens fixing frame 120 and a pressing metal jig 121. The lens fixing frame 120 is fixed to the printed circuit board 117 with an adhesive 119 so that the aspherical glass lens 118 may focus an image or images onto the sensor chip 111. The pressing metal jig 121 fixes the aspherical glass lens 118 to the lens fixing frame 120.

The semiconductor optical sensing apparatus thus constructed detects an image or images focused by the aspherical glass lens 118 on the sensor chip 111 through the transparent plate 116, and outputs the detected image signals through the lead frames 113. The semiconductor optical sensing apparatus works as an image sensor.

[4] Column 6, line 63 – Column 7, line36—

A semiconductor optical sensor chip 2 is bonded onto the bottom of a plastic casing 1. The sensor chip may be a CCD image sensor, an MOS image sensor, a photodiode, an ultraviolet ray sensor or such an optical sensor. The plastic casing 1 includes a bonding portion, on which the sensor chip 2 is bonded, a supporting portion for supporting the bonding portion, and openings 1a and 1b. The openings 1a and 1b are opened in the bottom of the plastic casing 1 except the bonding portion and the supporting portion.

Lead frames 3 as wiring means extend from the inside to the outside of the plastic casing 1. Internal terminals on the surface of the sensor chip 2 are connected to the lead frames 3 via bonding wires 4 as connecting means. A transparent plate 5 is adhered or welded to the upper circumference of the plastic casing 1. The transparent plate 5 is wide enough to completely cover the upper opening of the plastic casing 1.

Focusing means 6 is adhered or welded to the upper circumference of the transparent plate 5. The focusing means 6 includes a lens 6a and a frame 6b integrally formed therewith. The lens 6a is formed under an upper surface of the frame 6b. The lens 6a focuses an image or images onto the sensor chip 2. The plastic casing 1, the transparent plate 5 and the focusing means 6 are made of the same material. Or, the plastic

Discussion

casing 1, the transparent plate 5 and the focusing means 6 are made of materials, thermal expansion coefficients of which are almost the same. The reason for this will be described later.

The space inside the plastic casing 1 is filled with transparent silicone gel 7 as a transparent filler. The transparent silicone gel 7 is exposed outside through the openings 1a and 1b at the bottom of the plastic casing 1. According to the first embodiment, the transparent silicone gel 7 completely fills the space inside the plastic casing 1 in such a manner that the transparent silicone gel 7 completely seals and protects the sensor chip 2 and the bonding wires 4. Gas which adversely affects the semiconductor sensor chip is not used for sealing according to the first embodiment. Therefore, the characteristics of the semiconductor optical sensing apparatus are maintained stably according to the first embodiment.

[5] Column 8, lines 26-31—

Then, the plastic casing 1 with the other constituent elements 2, 5 and 6 assembled so far is turned upside down and transparent silicone gel 7 is injected through the openings 1a and 1b. The plastic casing 1 is placed in an oven and the transparent silicone gel 7 is cured thermally.

[6] Column 9, Lines 11-40—

FIG. 3(a) is a plan view of a semiconductor optical sensing apparatus according to a third embodiment of the invention. FIG. 3(b) is a cross sectional view taken along line 3b–3b of FIG. 3(a). The semiconductor optical sensing apparatus according to the third embodiment has an external appearance as shown in FIG. 19(c).

The semiconductor optical sensing apparatus according to the third embodiment has a structure excluding the transparent plate 5 from the semiconductor optical sensing apparatus according to the first embodiment, and focusing means 6 is directly adhered or welded to the plastic casing 1. As shown in FIG. 19(c), the focusing means 6 is shaped with a parallelepiped or rectangular form, that is wide enough to completely cover the upper opening of a plastic casing 1. A lens 6a is configured such that its focal point is positioned always on a semiconductor optical sensor chip 2.

The plastic casing 1 and the focusing means 6 are made of the same material or materials having almost the same thermal expansion coefficients.

The focal point of the lens 6a is positioned always on the semiconductor optical sensor chip 2 even when the plastic casing 1 and the focusing means 6 expand or contract thermally. Openings 1a and 1b absorb the volume change of the transparent silicone gel 7 due to the thermal expansion or contraction such that stable sealing is maintained. Thus, the semiconductor optical sensing apparatus according to the third embodiment exhibits high detection capability even in the environments in which the temperature changes sharply or widely.

FIG. 4(a) is a plan view of a semiconductor optical sensing apparatus according to a fourth embodiment of the invention. FIG. 4(b) is a cross sectional view taken along line 4b–4b of FIG. 4(a). The semiconductor optical sensing apparatus according to the fourth embodiment has an external appearance as shown in FIG. 19(c).

Claim 1, as amended, recites

> *A package for an imager integrated circuit chip, the imager integrated circuit chip having a bond pad for communicating an electrical signal to or from the imager integrated circuit chip, the package comprising:*
>
> *a printed circuit board comprising:*
>
> *multiple routing layers including a plurality of bond leads and a plurality of package leads, wherein at least one package lead is electrically coupled to at least one bond lead; and*
>
> *at least one of the multiple routing layers comprising a ground plane;*
>
> *the imager integrated circuit chip disposed on the printed circuit board and coupled to at least one of the plurality of bond leads to thereby allow communication of the electrical signal between the at least one package lead and the imager integrated circuit chip; and*
>
> *an optical cover, disposed on the printed circuit board, that, with the printed circuit board, encapsulates the imager integrated circuit chip.*

Specifically, amended claim 1 is directed to a package for an imager integrated circuit chip package. The package is a multi-layer package characterized by multiple routing layers including a plurality of bond leads and a plurality of package leads, where at least one package lead is electrically coupled to at least one bond lead. At least one of the multiple routing layers is a ground plane.

The integrated circuit chip includes an imager component comprising the multilayer printed circuit board, above, an imager integrated circuit chip, and an optically transmissive material deposited on the imager integrated circuit chip.

Neither of the references show a multi-layer substrate.

Knapp '337 describes a semiconductor device that is coupled to a ball grid array substrate and encapsulated by an optically transmissive material. The ball grid array substrate has conductive interconnects and a semiconductor receiving area on a top surface and solder pads on a bottom surface. The optoelectronic component is mounted on the semiconductor receiving area and encapsulated with the optically transmissive material.

Solder balls are formed on the solder pads. To be noted is that the substrate (11) is a single layer, and does not have internal circuitization. Knapp et al. shows traces 12 and 14 in Figures 1, 2, 3, and 4. But, these are mere "traces" and not applicant's "*multiple routing layers including a plurality of bond leads and a plurality of package leads, wherein at least one package lead is electrically coupled to at least one bond; and at least one of the multiple routing layers comprises a ground plane...*"

Claim 10 recites "a preformed package base comprising:

> *an insulating substrate comprising multiple routing layers including a plurality of bond leads and a plurality of package leads electrically coupled to the plurality of bond leads, wherein at least one package lead is electrically coupled to the at least one bond lead; and*
> *at least one of the multiple routing layers comprises a ground plane;*
> *a plurality of bond leads disposed on the insulating substrate, and*
> *a plurality of package leads electrically coupled to the plurality of bond leads:*

where the claimed "multiple routing layers including a plurality of bond leads and a plurality of package leads wherein at least one package lead is electrically coupled to the at least one bond lead; and at least one of the multiple routing layers comprises a ground plane" is neither taught nor suggested by Knapp et al.'s traces 12 and 14 in Figures 1, 2, 3, and 4.

Claim 18 recites

> *a printed circuit board comprising*
> *a) multiple routing layers, a plurality of bond leads and a plurality of package leads;*
> *b) at least one of the multiple routing layers comprising a ground-plane,*
> *c) at least one of the plurality of bond leads coupled to at least one of the plurality of package leads;*
> *at least one of the plurality of bond leads coupled to at least one of the plurality of package leads;*

which is neither taught nor suggested by Knapp et al.'s traces 12 and 14 in Figures 1, 2, 3, and 4.

Fukamura '872 describes a semiconductor optical sensing apparatus having a casing made of an electrically insulative material and with at least one opening at a bottom portion; a wiring device extending from an inside to an outside of the casing; a

semiconductor optical sensor chip bonded to the bottom portion of the casing; and a connecting device for connecting a terminal of the sensor chip and the wiring device.

Fukamura describes a transparent filler is filled in a space inside the casing to cover the sensor chip. The opening absorbs a volume change of the transparent filler caused by expansion or contraction. A focusing device is connected to the casing and located at a position to focus an image on the sensor chip. The focusing device and casing are made of the same material or materials having substantially same thermal expansion coefficients.

The semiconductor apparatus is characterized by Fukamura as "a simple structure less affected by temperature variations" and is said to facilitate preventing deterioration and variation of optical characteristics, elongating life and improving reliability of the apparatus. But this is a single layer structure without interplanar circuitization.

The portion of Fukamura et al. describing Figures 20(a) and 20(b) is at column 1, lines 34-44,

> *Referring now to FIGS. 20(a) and 20(b), the semiconductor optical sensing apparatus includes a detecting section and an optical section. The detecting section includes a semiconductor optical sensor chip 111, a ceramic casing 112, lead frames 113, bonding wires 114 and a transparent plate 116. The sensor chip 111 is die-bonded to the casing 112. The lead frames 113 include lead pins. The bonding wires 114 connect the internal terminals of the sensor chip 111 and the lead frames 113. The transparent plate 116 is fixed to the open end of the casing 112 with a layer 115 of glass having a low melting point or of adhesive.*

While the portion of Fukamura describing Figures 3(a) and 3(b) is at column 9, lines 11-40,

> *FIG. 3(a) is a plan view of a semiconductor optical sensing apparatus according to a third embodiment of the invention. FIG. 3(b) is a cross sectional view taken along line 3b--3b of FIG. 3(a). The semiconductor optical sensing apparatus according to the third embodiment has an external appearance as shown in FIG. 19(c).*
>
> *The semiconductor optical sensing apparatus according to the third embodiment has a structure excluding the transparent plate 5 from the semiconductor optical sensing apparatus according to the first embodiment, and focusing means 6 is directly adhered or*

welded to the plastic casing 1. As shown in FIG. 19(c), the focusing means 6 is shaped with a parallelepiped or rectangular form, that is wide enough to completely cover the upper opening of a plastic casing 1. A lens 6a is configured such that its focal point is positioned always on a semiconductor optical sensor chip 2.

The plastic casing 1 and the focusing means 6 are made of the same material or materials having almost the same thermal expansion coefficients.

The focal point of the lens 6a is positioned always on the semiconductor optical sensor chip 2 even when the plastic casing 1 and the focusing means 6 expand or contract thermally. Openings 1a and 1b absorb the volume change of the transparent silicone gel 7 due to the thermal expansion or contraction such that stable sealing is maintained. Thus, the semiconductor optical sensing apparatus according to the third embodiment exhibits high detection capability even in the environments in which the temperature changes sharply or widely.

Neither Fukamura generally, nor the two cited portions of Fukamura teach or suggest Applicant's claim limitations of Claim 1:

a printed circuit board comprising:

multiple routing layers including a plurality of bond leads and a plurality of package leads, wherein at least one package lead is electrically coupled to at least one bond lead; and

at least one of the multiple routing layers comprising a ground plane;

or of Claim 10 which recites "a preformed package base comprising:

an insulating substrate comprising multiple routing layers including a plurality of bond leads and a plurality of package leads electrically coupled to the plurality of bond leads, wherein at least one package lead is electrically coupled to the at least one bond lead; and
at least one of the multiple routing layers comprises a ground plane;
a plurality of bond leads disposed on the insulating substrate, and
a plurality of package leads electrically coupled to the plurality of bond leads:

or of Claim 18 which recites

a printed circuit board comprising
a) multiple routing layers, a plurality of bond leads and a plurality of package leads;
b) at least one of the multiple routing layers comprising a ground-plane,
c) at least one of the plurality of bond leads coupled to at least one of the plurality of package leads;
at least one of the plurality of bond leads coupled to at least one of the plurality of package leads;

Neither of the references shows the multilayer construction with interplanar circuitization.

Neither Knapp nor Fukamura teach or suggest the structure claimed by Applicants, and the claims are properly allowable to Applicants.

Conclusion

Based on the above discussion, it is respectfully submitted that the pending claims describe an invention that is properly allowable to the Applicants.

If any issues remain unresolved despite the present amendment, the Examiner is requested to telephone Applicants' Attorney at the telephone number shown below to arrange for a telephonic interview before issuing another Office Action.

Applicants would like to take this opportunity to thank the Examiner for a thorough and competent examination and for courtesies extended to Applicants' Attorney.

The Commissioner is hereby authorized to charge any additional fees due or credit any overpayment to Deposit Account No. 50-2421.

Respectfully Submitted

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